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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/419,439	10/15/1999	THOMAS D. HARTNETT	RA-5274	1274

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EXAMINER	
WOOD, WILLIAM H	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/419,439	HARTNETT ET AL.	
	Examiner	Art Unit	
	William H. Wood	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-15 and 19-22* is/are rejected.

7)☒ Claim(s) *8-11 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *October 15, 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Patent Office Communiqué

This detailed action is directed to the acknowledgement of the patent office receiving and beginning an examination of patent application, "Pipeline Depth Controller for an Instruction Processor" (patent office application number: 09/419,439), being filed on October 15, 1999 and being assigned to Patent Examiner William Wood.

Acknowledgement is made of patent office receiving paper, "Associate Power of Attorney", being filed on March 22, 2000.

Drawings

1. The drawings are objected to because Figure 10, part 354 is cut off at the end of the timing diagram. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because it exceeds the maximum allowable length of 150 words. Correction is required. See MPEP § 608.01(b).

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. It is suggested to remove the phrase "pipeline depth" and more aptly describe the conditions as to how the pipeline fill is controlled.

Claim Objections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 11-18 are objected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In regard to claim 11, while applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "pipeline depth" in claims 11-15 and 18 is used by the claim to mean "number of instructions entering the pipeline," while the accepted meaning is "number of stages composing the pipeline." A better suited term would be "pipeline fill."

In regard to claims 12-18, the claims are dependent on objected base claims and as such included the same faulty clarity in subject matter and therefore, are objected to as well.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application

being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 11, 13 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Zaidi et al. (USPN 5,996,064) filed December 30, 1997.

In regard to claim 1, Zaidi taught the following limitations of the claim:

i) *For use in a data processing system having an instruction processor to execute instructions included in the instruction set of the instruction processor, the instruction processor having an instruction pipeline* (column 1, lines 4-11) *capable of initiating simultaneous execution on a variable number of the instructions* (column 5, line 66 to column 6, line 6; the scheduling allows for a variable number of instructions) *in a predetermined period of time* (the length of the pipeline itself determines the predetermined period of time), *a system for programmably controlling the variable number of the instructions beginning execution within the instruction pipeline during the predetermined period of time* (column 5, line 66 to column 6, line 6)

ii) *a first storage device to receive and to store a programmable count value* (Figure 3, part 40)

iii) *a logic sequencer coupled to the first storage device to receive the programmable count value* (Figure 3, part 42), *and in response thereto, to generate a pipeline control signal provided to the instruction pipeline to cause the*

instruction pipeline to receive, and to initiate concurrent execution on, a predetermined number of the instructions (column 6, lines 7-13; scheduler determines the number of instructions to allow into the pipeline based on the post-ready latency value) *in the predetermined period of time* (the length of the pipeline) *as determined by the programmable count value* (post-ready latency value).

In regard to claim 11, Zaidi taught the following limitations of the claim:

i) *For use in an instruction pipeline of an instruction processor, the instruction processor to execute instructions that are part of the instruction set of the instruction processor, the instruction pipeline being adapted to initiate the execution of a variable number of instructions, up to a predetermined maximum number of instructions* (predetermined number based on the stages of the pipeline), *within a predetermined period of time when the instruction pipeline is operating in a default mode* (time based on how long it takes an instruction to transverse through the pipeline; default mode is pushing in as many instructions as possible, ie. the number of stages), *and whereby up to the predetermined maximum number of instructions may be executing simultaneously within the instruction pipeline* (base on the previous two points), *the instructions pipeline including a pipeline depth controller to generate a pipeline control signal for temporarily preventing ones of the instructions from entering the instruction pipeline* (column 6, lines 7-13; scheduling is the "pipeline depth" controller), *a method of utilizing the pipeline depth controller to control the number of*

instructions for which execution is initiated by the instruction pipeline within the predetermined period of time (column 6, lines 7-13; controlled by the post-ready latency value, determines many instructions to let in the pipeline)

ii) *providing a count to the pipeline depth controller* (column 8, lines 48-52; counters 40 are inside the "pipeline depth" controller or scheduler; count is determined by the post-ready latency value)

iii) *utilizing the pipeline depth controller to selectively assert the pipeline control signal to cause the instruction pipeline to initiate the execution of the number of instructions specified by the count within a period of time equal to the predetermined period of time* (signal is set by scheduler which is dependent on the post-ready latency value to allow only so many instructions into the pipeline at a time).

In regard to claim 13, Zaidi taught the additional further limitations:

i) *wherein the instruction processor includes a first memory device coupled to the pipeline depth controller* (Figure 4B, and column 8, lines 48-52)

ii) *with the step, storing within the first memory device respective first count signals for each of the first predetermined ones of the instructions* (Figure 4B; post-ready latency field)

iii) *with the step, providing the respective first count signals to the pipeline depth controller as the count when a respective one of the first predetermined ones of the instructions enters the instruction pipeline* (column 8, lines 48-52).

In regard to claim 19, the limitations were taught by Zaidi as follows:

i) *For use in an instruction processor having an instruction pipeline for executing multiple instructions concurrently* (Figure 3, part 30), *the instruction pipeline being capable of initiating concurrent execution for up to a predetermined maximum number of instructions* (maximum number based on the length of the pipeline) *within a predetermined period of time* (time determined on how long it takes an instruction to move through pipeline based on its length), *a system for programmably controlling the number of instructions for which concurrent execution is initiated within the predetermined period of time* (column 6, lines 7-13)

ii) *storage means for receiving programmable count signals* (Figure 3, part 40)

iii) *sequencer means for responding to the programmable count signals* (Figure 3, part 42; scheduler), *and for issuing a pipeline control signal to the instruction pipeline for controlling the entry of instructions into the instruction pipeline* (column 6, lines 7-13; scheduler must signal only so many instructions based on the post-ready latency value) *such that concurrent execution is initiated for the number of instructions specified by the programmable count signals within a period of time equal to the predetermined period of time* (column 6, lines 7-13; the scheduler is allowing only so many instructions based on the post-ready latency value into the pipeline, which by default determines the predetermined time).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 5, 6, 12, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi et al. (USPN 5,996,064) in view of Naini et al. (USPN 6,209,083) filed on October 1, 1997.

In regard to claim 2, Zaidi taught the limitations of the previous claim 1. Zaidi did not teach *further including programmable enable logic to selectively enable the logic sequencer to be responsive to the programmable count value*. The enable logic portion of this limitation can be interpreted as simply a mode switch. As an example, the logic sequencer is either enabled to operate (mode 1), or it is not (mode 2). With this in mind it is important to note Naini taught a pipeline with multiple modes (column 1, line 66 to column 2, line 15), which has the advantage of reducing pipeline conflict (column 1, lines 56-62). Naini reduces pipeline conflict by evaluating the floating-point instructions. Monitoring certain types of instructions for conflict (such as dependencies and misprediction and so forth) is a well known concept. Motivated by a desire to reduce instruction conflict in pipelines, it would have been obvious to one of ordinary skill in the art to implement Zaidi's instruction issuing count system with Naini's ability to have multiple modes of operation depending on the instructions entering the pipeline. Thus, the combination of Zaidi and Naini taught enable logic (multiple modes) to make the

logic sequencer (scheduler) responsive to the count value (in other words activating this function).

In regard to claim 5, Zaidi taught the preceding limitations of claim 1 and the following limitation:

i) *to initiate execution of the predetermined number of the instructions during successive periods of time that are each equal to the predetermined period of time* (as long as the scheduler encounters the same instructions the successive periods of time will be the same)

Zaidi did not teach the following although Naini did:

ii) *further including scan enable logic* (the is the mode switch concept similar to above in claim 2's rejection, but here used for a different purpose)

iii) *coupled to the logic sequencer to programmably enable the logic sequencer to repeatedly generate the pipeline control signal* (this is the different purpose, which Zaidi will perform over and over due to the fact it gives no indication of ever not doing this)

The enable logic portion of this limitation can be interpreted as simply a mode switch though for a different purpose than above for claim 2. As an example, the logic sequencer is either enabled to repeatedly generate a signal (mode 1), or it is not (mode 2). With this in mind it is important to note Naini taught a pipeline with multiple modes (column 1, line 66 to column 2, line 15), which has the advantage of reducing pipeline conflict (column 1, lines 56-62). Naini reduces pipeline conflict by evaluating the floating-point instructions. Monitoring certain types of instructions for conflict (such as

dependencies and misprediction and so forth) is a well known concept. Motivated by a desire to reduce instruction conflict in pipelines, it would have been obvious to one of ordinary skill in the art to implement Zaidi's instruction issuing count system with Naini's ability to have multiple modes of operation. Thus, the combination of Zaidi and Naini taught enable logic (multiple modes) to make the logic sequencer (scheduler) responsive to the count value (in other words activating this function).

In regard to claim 6, Zaidi and Naini taught the preceding limitations as discussed above. Zaidi and Naini taught the additional limitations as follows:

i) *wherein the first storage device is adapted to receive, and to store, a respective first one of the programmable count values for each of first selectable ones of the instructions* (column 8, lines 47-53)

ii) *wherein the programmable enable logic includes circuits to enable the logic sequencer to receive, for any of the first selectable ones of the instructions, the respective first one of the programmable count values when any of the first selectable ones of the instructions enters the instruction pipeline to being execution*. The limitation of having enable logic to allow the sequencer to function is essentially the same as for claim 2 and therefore, rejected with a similar argument. The sequencer (or scheduler in Zaini) naturally performs the rest of these limitations as shown above.

In regard claim 12, this claim is similar to above claim 5 only being directed toward a different base claim. The same argument still applies to *enable circuit* (or as

above *scan enable logic*). The same argument still applies to the limitation *repeatedly assert a control signal* (or as above *repeatedly generate*).

In regard to claim 14, Zaidi taught the preceding limitations of the claim, however the additional limitation *programmably enabled* was not found in Zaidi, but in Naini. Furthermore, the limitation *programmably enabled* was shown to be combined in the rejection for claim 2 above and as such is done so here as well.

In regard to claim 20, this is similar to claims 5 and 12 above and as such is rejected in a similar manner. The only notable difference being the claims are all directed toward different base claims, however all the base claims have been rejected as well.

7. Claims 3, 4, 7, 15, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi et al. (USPN 5,996,064) in view of Naini et al. (USPN 6,209,083) in further view of Grochowski et al. (USPN 5,475,824) patented on December 12, 1995.

In regard to claim 3, Zaidi and Naini taught the preceding limitations:

i) *wherein the first storage device is coupled to receive a respective programmable count value* (found rejected above under claim 1)

ii) *and wherein the programmable enable logic includes circuits to selectively enable the logic sequencer to be responsive to the respective programmable count value* (found rejected above under claim 2)

The only limitation which was not taught by Zaidi and Naini was *system being responsive to predetermined combinations of the instructions entering the pipeline*,

however this limitation was found in Grochowski (column 4, lines 28-39). Grochowski further states the advantage of having paired combinations of instructions as being able to improve speed of execution (column 1, lines 10-15). However, a more related advantage to Zaidi is found in column 2, lines 21-29. Here Grochowski states a feature of the invention is determining the relationship of instructions (such as dependency) and then issuing the instructions accordingly. This would aid Zaidi who himself mentions dependency detection (column 8, lines 22-25). Therefore, motivated by a need to determine relationships between instructions to increase speed of performance, it would have been obvious to one of ordinary skill in the art to implement Zaidi with the teachings of Grochowski to have paired predetermined combinations of instructions.

In regard to claim 4, Zaidi and Naini taught the preceding limitations as discussed above. Though this claim is not dependent on claim 3, Grochowski is included in the grounds of rejection to overcome the limitation of *predetermined combinations of instructions*, which has been included in this claim. For this limitation the reasoning is the same as above for claim 3. With regard to the additional limitation *wherein logic responsive to count value only if a predetermined condition occurs within the instruction pipeline* this is clearly read upon by as the predetermined pipeline condition simply being the existence of the instruction pair combination.

In regard to claim 7, Zaidi taught the additional limitations:

i) *a second storage device coupled to the first storage device to store each respective first one of programmable count values and to provide each respecitive first one of programmable count values to first storage device as a*

respective one of first selectable ones of the instructions enters the instruction pipeline (Figure 4B, part 60; this is the second storage device, the Post-Ready Latency field stores the programmable count values).

ii) *second storage device further to store respective first instruction combination signals for each of first selectable ones of instructions* (Figure 4B, part 60; Scheduler Information field is the combination signals part).

Zaidi did not teach the limitations though Grochowski did:

i) *a third storage device coupled to logic sequencer, third storage device adapted to store respective second instruction combination signals for each of second selectable ones of the instructions.*

ii) *a compare circuit to enable logic sequencer to be responsive to respective first one of programmable count values for an executing one of the instructions N+1 where instruction N+1 is one of first selectable ones of the instructions and if respective first instruction combination signals for instruction N+1 have a predetermined relationship to respective second instruction combination signals for one of the instructions N wherein instruction N is one of second selectable ones of the instructions, and is further in the instruction to enter the instruction pipeline immediately before instruction N+1.*

These two limitations are interpreted as basically saying a storage device to store second instruction combination signals in order to determine (with the aid of the first instruction combination signals) if a pair of sequential instructions introduces a condition into the pipeline that would necessitate using the programmable count values. This

concept of pairing instructions for a predetermined condition (execution in parallel) is found in Grochowski (column 2, lines 8-20). Grochowski taught one storage device for one set of instructions and one storage device for a second set of instructions (column 4, lines 2-6; two criteria must be met, and therefore some storage device must be maintained for both conditions to be tested). These instructions are subsequent in instruction stream order (column 4, lines 7-11). Grochowski mentions this increases efficiency by way of increasing speed (column 1, lines 19-23), but only if certain conditions are met, such as dependency detection (column 1, lines 54-58), which is advantageous to Zaidi who needs to determine instruction relationships in order to issue instructions correctly. Grochowski would be combined with Zaidi in so much as Zaidi already has the first half of the pair of storage devices as mentioned above, but needs a way of tracking the second instruction sequence (Grochowski's two instruction monitoring system). Finally, Zaidi alludes to a dependency checking system (column 4, lines 23-25). Therefore, motivated by a desire to efficiently process an instruction stream searching for pairs that reveal a certain condition, it would have been obvious to one of ordinary skill in the art to implement Zaidi in light of Grochowski.

In regard to claim 15, Zaidi taught the limitations as follows:

i) *storing within the first memory device respective first compare signals for each of the first predetermined ones of the instructions* (Figure 4B, part 60; Scheduler Information field is the compare signals part as it is used to identify the instructions for what is to be done with those instructions)

Zaidi did not however teach the following limitations, but they can be found in Naini:

ii) *instruction processor includes a second memory device coupled to the pipeline depth controller*

iii) *storing within the second memory device respective second compare signals for each of second predetermined ones of the instructions*

iv) *comparing said respective first compare signals for an instruction N+1 that is one of said first predetermined ones of the instructions and that is executing within the instruction pipeline to said respective second compare signals for an instruction N that is one of the second predetermined one so the instructions, and that entered the instruction pipeline for execution before said instruction N+1 entered the instruction pipeline, the comparing step performed to determine whether a predetermined relationship exists between the respective first compare signals for the instruction N+1 and the respective second compare signals for the instruction N*

v) *wherein the step of providing the respective first count signals to the pipeline depth controller is performed only if the predetermined relationship exists.*

The above limitations are interpreted as basically saying a storage device to store second instruction combination signals in order to determine (with the aid of the first instruction compare signals) if a pair of sequential instructions introduces a condition into the pipeline that would necessitate using the programmable count values. This concept of pairing instructions for a predetermined condition (execution in parallel) is found in Grochowski (column 2, lines 8-20). Grochowski taught one storage device for one set of instructions and one storage device for a second set of instructions (column

4, lines 2-6; two criteria must be met, and therefore some storage device must be maintained for both conditions to be tested). These instructions are subsequent in instruction stream order (column 4, lines 7-11). Grochowski mentions this increases efficiency by way of increasing speed (column 1, lines 19-23), but only if certain conditions are met, such as dependency detection (column 1, lines 54-58), which is advantageous to Zaidi who needs to determine instruction relationships in order to issue instructions correctly. Grochowski would be combined with Zaidi in so much as Zaidi already has the first half of the pair of storage devices as mentioned above, but needs a way of tracking the second instruction sequence (Grochowski's two instruction monitoring system). Finally, Zaidi alludes to a dependency checking system (column 4, lines 23-25). Therefore, motivated by a desire to efficiently process an instruction stream searching for pairs that reveal a certain condition, it would have been obvious to one of ordinary skill in the art to implement Zaidi in light of Grochowski.

In regard to claim 21, Zaidi and Naini taught the preceding limitations as discussed above. However, Zaidi and Naini did not teach *further including instruction combination means for providing respective ones of the programmable count signals to the storage means when an associated predetermined combination of the instructions has entered the instruction pipeline*. This can be found in Grochowski as the instruction pairing concept explained in claim 3 above and is rejected in a similar manner here only with relation to a different base claim.

In regard to claim 22, Zaidi, Naini and Grochowski taught the following limitation *responding to variable condition occurring within the instruction processor* (the variable

condition in this case is read upon by the existence of the paired instructions as taught by Grochowski above).

Allowable Subject Matter

8. Claims 8-10 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In regard to claims 8 and 9, the following is a statement of reasons for the indication of allowable subject matter: claims 8 and 9 are allowable over prior art of record because a reasonable search does not detect the combined limitations of the claim. Specifically, the prior art of record fails to teach the limitations or the motivation to recreate the limitations of claims 8 and 9 in such a manner as *wherein the third storage device further includes circuits to store microcode instructions to control execution of extended ones of the instructions predetermined ones of the microcode instructions being associated with associated ones of the respective second instruction combination signals a microsequencer coupled to the third storage device to read out a respective sequence of the microcode instructions to control execution of the respective one of the extended ones of the instructions that is being executed within the instruction pipeline and whereby if any of the microcode instructions are the predetermined ones of the microcode instructions, to provide the associated ones of the respective second instruction combination signals to the compare circuit as the respective second instruction combination signals for the instruction N.* And as such, claims 8 and 9 are allowable though objected to for being dependent to rejected claims.

In regard to claim 10, the following is a statement of reasons for the indication of allowable subject matter: claim 10 is allowable over prior art of record because a reasonable search does not detect the combined limitations of the claim. Specifically, the prior art of record fails to teach the limitations or the motivation to recreate the limitations of claim 10 in such a manner as *wherein the third storage device further includes circuits to store a respective second one of the programmable count values for each of the second selectable ones of the machine instructions, and further including a programmable selector coupled to the first storage device to programmably select between the respective second one of the programmable count values for the instruction N or the respective first one of the programmable count values for the instruction N+1 for use as the programmable count value.* And as such, claim 10 is allowable though objected to for being dependent to rejected claims.

In regard to claims 16 and 17, the following is a statement of reasons for the indication of allowable subject matter: claims 16 and 17 are allowable over prior art of record because a reasonable search does not detect the combined limitations of the claim. Specifically, the prior art of record fails to teach the limitations or the motivation to recreate the limitations of claim 16 and 17 in such a manner as *wherein the second memory device further stores microcode instructions to control the execution ofones of the instruction that are extended-mode instructions, and wherein the instruction processor includes a microsequencer to read a respective sequence of the microcode instructions from the second memory device to control execution of an instruction that is resident within the instruction pipeline, and further including the steps of: associating*

predetermined ones of the microcode instructions each with a respective one of the respective second compare signals; reading via the microsequencer the respective sequence of the microcode instructions from the second memory device for the instruction N when the instruction N is one of the extended mode instructions; performing the comparing step using the respective second compare signals that have been associated with any predetermined micro instruction included in the sequence of micro instructions. And as such, claims 16 and 17 are allowable though objected to for being dependent to rejected claims

In regard to claim 18, the following is a statement of reasons for the indication of allowable subject matter: claim 18 is allowable over prior art of record because a reasonable search does not detect the combined limitations of the claim. Specifically, the prior art of record fails to teach the limitations or the motivation to recreate the limitations of claim 18 in such a manner as *wherein the second memory device further stores respective second count signals for each of the second predetermined ones of the instructions, and wherein the step of providing the first respective count signals to the pipeline depth controller includes the step of selecting whether the respective second count signals will be substituted for use as second count instead of the first respective count signals.* And as such, claim 18 is allowable though objected to for being dependent to rejected claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to

a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Fukuda et al. (USPN 5,175,844) taught a method of controlling the rate of a processor's operation. This is applicable since applicant's invention is basically performing the same process.

Kuslak (USPN 5,911,083) taught another method of controlling the rate of a processor's operation. Additionally, Kuslak taught this as a programmable function. Kuslak further states directly the use of a count means to control the processor.

Solari et al. (USPN 5,617,576) taught a method of controlling the speed at which a processor operates.

Inoue (USPN 5,392,444) taught a programmable controller for completing certain instruction execution requirements.

Lansford (USPN 5,041,962) taught another method of controlling a microprocessor's speed.

Shiell et al. (USPN 6,138,232) taught a system of storing programmable processor rate controlling values in a table. The values being programmed to be placed in a count system by interrupts.

Lui et al. (USPN 5,964,863) taught a method of slowing the execution of a processor base on specific conditions found in the processor. Lui asserts certain signals to halt processor access to memory including the cache.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
May 6, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100